IGBTs, numerals **711** to **716** denote diodes, **801** to **806** denotes gate circuits, **900** denotes a P terminal, **901** an N terminal, **910**, **911** and **912** denote U, V and W terminals respectively, **920** a main circuit inductance, **950** a motor.

[0088] A feature of FIG. **12** lies in that the IGBTs of the structures explained in the embodiments 1 to 7 are applied to the IGBTs **701** to **706**. The inverter of FIG. **12**, to which the IGBTs of the embodiments 1 to 7 is applied, can have a low loss and a high reliability due to its IGBT effects.

[0089] The arrangement of the inverter of FIG. **12** is illustrated merely as an example. For example, when a switching element and a diode are connected in reverse parallel to form a parallel circuit, a pair of such parallel circuits are connected in series to form a series circuit, and such series circuits are provided to correspond in number to phases to form an inverter; the inverter can also have similar effects.

[0090] Although such an inverter as to convert a DC current to an AC current in the present embodiment, the present invention is not limited to this specific example. Thus it will be obvious to those skill in the art that even such a converter as to convert an AC current to a DC current can have similar effects.

[0091] It should be further understood by those skilled in the art that although the foregoing description has been made on embodiments of the invention, the invention is not limited thereto and various changes and modifications may be made without departing from the spirit of the invention and the scope of the appended claims.

1. A semiconductor device comprising:

a semiconductor substrate having a pair of main surfaces;

a first semiconductor region of a first conductivity type positioned adjacent to one of the main surfaces of the semiconductor substrate and located within the semiconductor substrate;

a second semiconductor region of a second conductivity type provided adjacent to the first semiconductor region and having a carrier concentration lower than a carrier concentration of the first semiconductor region;

a third semiconductor region of the second conductivity type provided adjacent to the second semiconductor region and having a carrier concentration lower than the carrier concentration of the second semiconductor region;

a plurality of MOS type trench gates extended from one of the main surfaces of the semiconductor substrate into the third semiconductor region to have at least two sorts of different intervals;

a fourth semiconductor region of the first conductivity type provided between the MOS type trench gates having a narrow adjacent interval and having a carrier concentration higher than the carrier concentration of the third semiconductor region;

a fifth semiconductor region of the second conductivity type provided between the MOS type trench gates having the narrow adjacent interval, located within the fourth semiconductor region to be adjacent to the MOS type trench gates, and having a carrier concentration higher than the carrier concentration of the fourth semiconductor region;

a sixth semiconductor region of the first conductivity type located between the MOS type trench gates having the narrow adjacent interval and having a carrier concentration higher than the carrier concentration of the third semiconductor region;

a first electrode located between the MOS type trench gates having the narrow adjacent interval to be contacted with the fourth and fifth semiconductor regions; and

a second electrode contacted with the first semiconductor region,

wherein the third semiconductor region is exposed to the main surface between the sixth semiconductor region and the trench gates.

2. A semiconductor device according to claim **1**, wherein the sixth semiconductor region is spaced from the trench gates by a distance not larger than 10 μm.

3. A semiconductor device according to claim **1**, wherein the sixth semiconductor region is deeper than the third semiconductor region.

4. A semiconductor device according to claim **1**, wherein the fourth semiconductor region is formed to cover a lower side of the trench gates.

5. A semiconductor device according to claim **1**, further comprising:

a seventh semiconductor region of the second conductivity type which is provided between the MOS type trench gates having the adjacent narrow interval, located between the third and fourth semiconductor regions to be adjacent to the MOS type trench gates, and has a carrier concentration higher than the carrier concentration of the third semiconductor region.

6. A semiconductor device according to claim **5**, further comprising:

an eighth semiconductor region of the first conductivity type which is located between the third and seventh semiconductor regions, contacted with the MOS type trench gates, and has a carrier concentration higher than the carrier concentration of the third semiconductor region.

7. A semiconductor device according to claim **1**, wherein the sixth semiconductor region is contacted with the first electrode directly or through a resistance.

8. A power converter comprising:

a pair of DC terminals;

AC terminals corresponding in number to phases of an AC source; and

a plurality of power conversion units connected between the pair of DC terminals,

wherein each of the power conversion units has a series circuit of two parallel circuits each having a switching element and a diode of a polarity opposite to the switching element, the power conversion units have the AC terminals as different mutual interconnection points between the two parallel circuits, and the switching element is the semiconductor device set forth in claim **1**.

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